

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1 1. (Currently Amended) A method for designing a programmable logic
2 device, the method comprising:
3 assigning each of a plurality of circuit elements to a separate abstract block,
4 wherein the circuit elements are part of a user design for a programmable integrated circuit and
5 ~~the~~ each abstract block represents a functional attribute of its assigned circuit element;
6 placing a respective one or more of the abstract blocks into each of a plurality of
7 logic blocks based at least in part on a correspondence between a functional attribute of a
8 particular logic block and the functional attribute of ~~an~~ a respective abstract block placed into
9 that logic block, wherein a first abstract block is placed into a first logic block, wherein placing a
10 respective one or more of the abstract blocks into each of a plurality of logic blocks includes:
11 determining whether placing an abstract block assigned to a particular
12 circuit element into a specific logic block violates any of a set of design rules relating to that
13 specific logic block, wherein the logic blocks are grouped into clusters; and
14 determining whether placing the abstract block into a cluster containing
15 that specific logic block violates any of a set of design rules relating to that cluster;
16 removing the first abstract block from the first logic block in response to
17 placement information that indicates a design goal would be improved by rearranging at least a
18 portion of the user design, wherein the design goal includes at least one of routability and signal
19 timing in the user design; and
20 placing the first abstract block into a second logic block on the programmable
21 integrated circuit, wherein the functional attribute of the first abstract block corresponds with a
22 functional attribute of the second logic block, thus improving the design goal.

2. (Currently Amended) The method according to claim 1 wherein the design goal includes both routability and signal timing in the user design.

3. (Original) The method according to claim 1 wherein the circuit elements include lookup tables and registers.

4. (Original) The method according to claim 1 wherein the circuit elements include DSP blocks and RAM blocks.

5. (Canceled)

6. (Currently Amended) The method according to claim ~~5-1~~ wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of nets and connections of nets absorbed into the cluster if the abstract block is placed inside the cluster.

7. (Currently Amended) The method according to claim ~~5-1~~ wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of timing critical connections absorbed into the cluster if the abstract block is placed inside the cluster.

8. (Currently Amended) The method according to claim ~~5-1~~ wherein placing a respective one or more of the abstract blocks into each of a plurality of logic blocks further ~~comprises~~includes:

placing the abstract block into another logic block within the same cluster if placing that abstract block into that specific logic block violates any of the design rules relating to that specific logic block; and

placing the abstract block into another cluster if placing that abstract block into that cluster violates any of the design rules relating to that cluster.

1 9. (Previously Presented) The method according to claim 1 wherein the
2 logic blocks implement functions performed by two lookup tables with less than an integer k
3 unique input variables; and the method further comprises:
4 determining whether placing an abstract block into a logic block causes that logic
5 block to have more than k unique input variables.

1 10. (Original) The method according to claim 1 wherein the placement
2 information includes floorplanning information.

1 11. (Original) The method according to claim 1 wherein the placement
2 information includes partition information.

1 12. (Previously Presented) The method according to claim 1 wherein the
2 placement information includes data obtained by a previous placement of a portion of the user
3 design on the programmable integrated circuit.

1 13. (Canceled)

1 14. (Currently Amended) A computer program product stored on a computer
2 readable medium encoded with computer program instructions for controlling operation of a
3 computer system for designing a programmable integrated circuit, the computer program product
4 comprising:

5 computer program instructions for assigning each of a plurality of circuit elements
6 to a separate abstract block, wherein ~~the~~ each abstract block represents a functional attribute of
7 its assigned circuit element;

8 computer program instructions for placing a respective one or more of the abstract
9 blocks into each of a plurality of logic blocks based at least in part on a correspondence between
10 a functional attribute of a particular logic block and the functional attribute of ~~an~~ a respective
11 abstract block placed into that logic block, wherein a first abstract block is placed into a first
12 logic block, wherein the logic blocks are grouped into clusters of logic blocks, and wherein the

computer program instructions for placing a respective one or more of the abstract blocks into each of a plurality of logic blocks includes:

computer program instructions for determining whether placing the abstract blocks into the clusters violates any design rules of the clusters; and

computer program instructions for determining whether placing the abstract blocks into the logic blocks violates any design rules of the logic blocks;

computer program instructions for determining whether placement information indicates that a design goal would be improved by moving at least one of the abstract blocks into a different logic block, wherein the design goal includes at least one of routability and signal timing in the user design; and

computer program instructions for removing the first abstract block from a first logic block and placing the first abstract block into a second logic block in response to the determination based on the placement information, wherein the functional attribute of the removed first abstract block corresponds with a functional attribute of the second logic block.

15. (Currently Amended) The computer program product as defined in claim 14 wherein the design goal includes both signal timing and routability in the user design.

16. (Currently Amended) The computer program product as defined in claim 14 ~~wherein the logic blocks are grouped into clusters of logic blocks, and the computer program instructions for placing a respective one or more of the abstract blocks into each of a plurality of logic blocks further comprises, further comprising~~ computer program instructions for grouping each of the abstract blocks into a cluster of logic blocks based on an attraction of the abstract block to the cluster.

17. (Canceled)

18. (Original) The computer program product as defined in claim 14 wherein some of the circuit elements are lookup tables, and some of the circuit elements are registers.

1 19. (Original) The computer program product as defined in claim 16 wherein
2 the attraction measures a number of nets and connections of nets absorbed into the cluster if the
3 abstract block is placed inside the cluster.

1 20. (Original) The computer program product as defined in claim 16 wherein
2 the attraction measures a number of timing critical connections absorbed into the cluster if the
3 abstract block is placed inside the cluster.

1 21. (Previously Presented) The computer program product as defined in claim
2 17 further comprising:
3 computer program instructions for placing one of the abstract blocks into another
4 logic block if placing that abstract block to the logic block violates any of the design rules
5 relating to the logic block in which that abstract block was first placed.

1 22. (Previously Presented) The computer program product as defined in claim
2 17 further comprising:
3 computer program instructions for placing one of the abstract blocks to another
4 cluster if placing that abstract block to the first cluster violates any of the design rules relating to
5 the first cluster.

1 23. (Previously Presented) The computer program product as defined in claim
2 14 further comprising:
3 computer program instructions for determining whether placing the abstract
4 blocks into the logic blocks causes any of the logic blocks to have more than k unique input
5 variables,
6 wherein the logic blocks are configurable to implement functions performed by
7 two lookup tables with less than k unique input variables.

1 24. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes floorplanning information.

1 25. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes partition information.

1 26. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes data obtained by placing logic blocks that implement
3 portions of the user design on the programmable integrated circuit.

1 27. (Previously Presented) The method of claim 1, wherein each logic block
2 includes a first functional attribute and a second functional attribute, and wherein placing each of
3 the abstract blocks into a logic block further comprises:

4 assigning the first abstract block associated with a first circuit element to the first
5 functional attribute of the first logic block; and

6 assigning a second abstract block associated with a second circuit element to the
7 second functional attribute of the first logic block, such that the first logic block is assigned the
8 functional attributes of the first and second circuit elements.

1 28. (Previously Presented) The method of claim 27, wherein the first
2 functional attribute of the logic block includes a register and the functional attribute of the first
3 circuit element includes a register.

1 29. (Previously Presented) The method of claim 27, wherein the second
2 functional attribute of the logic block includes a look-up table circuit adapted to implement a
3 logic function and the functional attribute of the first circuit element includes a logic function
4 capable of being implemented by the look-up table circuit.

1 29. (Previously Presented) The method of claim 1 wherein a second abstract
2 block is placed into the first logic block prior to removing the first abstract block.